BASIC CHARACTERISTICS

FAMILY	OPERATING TEMPERATURE RANGE	VCC (V) min.	VCC (V) max.
CDB ... E	0 oC ... + 70 oC	4.75	5.25
CDB ... EM	-55 oC ... + 125 oC	4.50	5.50
CDB ... HE	0 oC ... + 70 oC	4.75	5.25
CDB ... HEM	-55 oC ... + 125 oC	4.50	5.50
74 LS ...	0 oC ... + 70 oC	4.75	5.25
54 LS ...	-55 oC ... + 125 oC	4.50	5.50
FZH 101 ... 171	0 oC ... + 70 oC	13.5	17
FZH 105 ... 175	-25 oC ... + 85 oC	13.5	17

BASIC CHARACTERISTICS PER NAND GATE

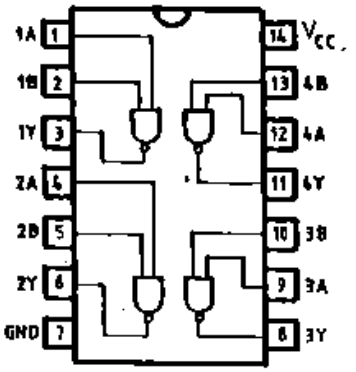
PARAMETER / FAMILIES	TTL CDB ...	TTL-H CDB...H	TTL-LS 54/74LS..	HLL FZH ...	Unit
VIH min	2	2	2	7.5	V
VIL max	0.8	0.8	0.7/0.8	4.5	V
IIH max	40	50	20	1	uA
- IIL max	1.6	2	0.4	1.8	mA
VOL max	0.4	0.4	0.4/0.5	1.7	V
VOH min	2.4	2.4	2.5/2.7	12	V
IOL min	16	20	4/8	18	mA
- IOH min	0.8	1	0.4	0.1	mA
IOS	18...55	40...100	15...100	15...60	mA
ICC typ @ VOL	3	6.5	0.6	3	mA
ICC typ @ VOH	1	2.5	0.2	1	mA
- VIK max	1.8	1.8	1.5	-	V
Pd medium	10	22	2	30	mW
tpLH typ	12	6	9	175	ns
tpHL typ	8	6.5	10	175	ns

QUADRUPLE 2-INPUT NAND GATES

CDB 400 EM
CDB 400 E

CDB 400 HEM
CDB 400 HE

* 54 LS 00
74 LS 00



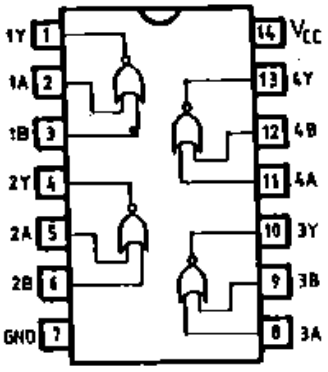
$Y = \overline{A.B}$

PACKAGE TO-116 / TOP VIEW

QUADRUPLE 2-INPUT NOR GATES

CDB 402 EM
CDB 402 E

* 54 LS 02
74 LS 02



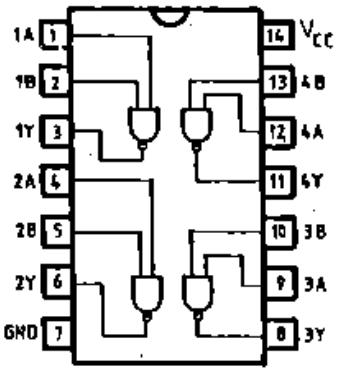
$Y = \overline{A+B}$

PACKAGE TO-116 / TOP VIEW

QUADRUPLE 2-INPUT NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

CDB 403 EM
CDB 403 E

* 54 LS 03
74 LS 03



$Y = \overline{A.B}$

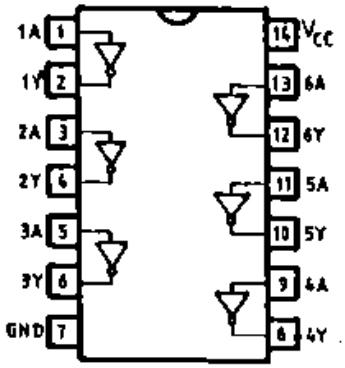
PACKAGE TO-116 / TOP VIEW

* Preliminary data

HEX INVERTERS

CDB 404 EM
CDB 404 E

$ 54 LS 04
$ 74 LS 04



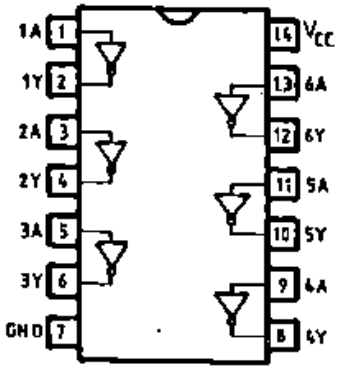
$Y = \overline{A}$

PACKAGE TO-116 / TOP VIEW

HEX INVERTERS
WITH OPEN-COLLECTOR OUTPUTS

CDB 405 EM
CDB 405 E

$ 54 LS 05
$ 74 LS 05

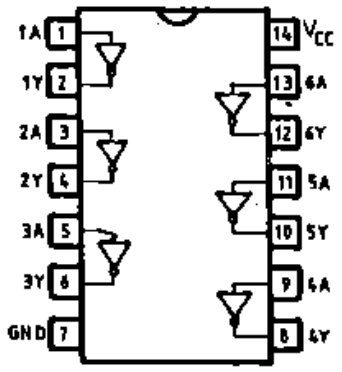


$Y = \overline{A}$

PACKAGE TO-116 / TOP VIEW

HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS (30 V)

CDB 406 EM
CDB 406 E



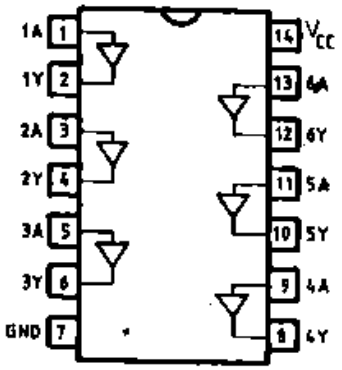
$Y = \overline{A}$

PACKAGE TO-116 / TOP VIEW

$ Preliminary data

HEX BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS (30 V)

CDB 407 EM
CDB 407 E



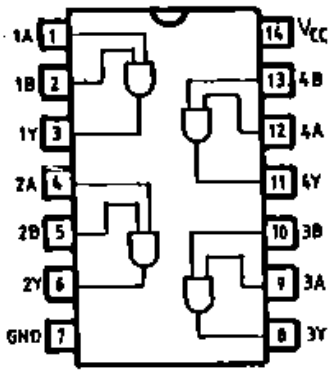
Y = A

PACKAGE TO-116 / TOP VIEW

QUADRUPLE 2-INPUT AND GATES

CDB 408 EM
CDB 408 E

$ 54 LS 08
74 LS 08



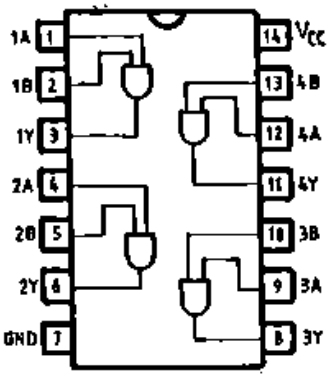
Y = A.B

PACKAGE TO-116 / TOP VIEW

QUADRUPLE 2-INPUT AND GATES
WITH OPEN-COLLECTOR OUTPUTS

CDB 409 EM
CDB 409 E

$ 54 LS 09
74 LS 09



Y = A.B

PACKAGE TO-116 / TOP VIEW

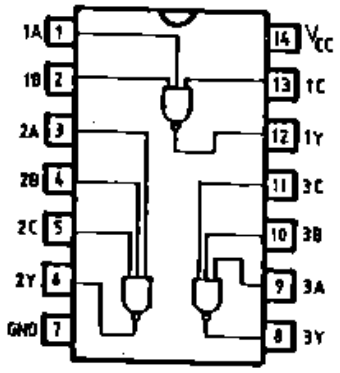
$ Preliminary data

TRIPLE 3-INPUT NAND GATES

CDB 410 EM
CDB 410 E

CDB 410 HEM
CDB 410 HE

* 54 LS 10
74 LS 10



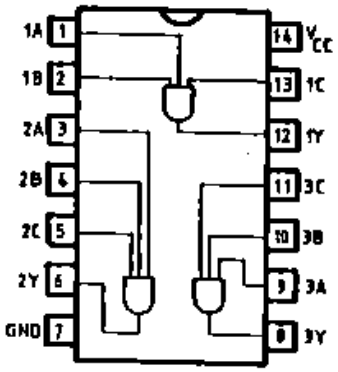
$Y = \overline{A.B.C}$

PACKAGE TO-116 / TOP VIEW

TRIPLE 3-INPUT AND GATES

CDB 411 HEM
CDB 411 HE

* 54 LS 11
74 LS 11

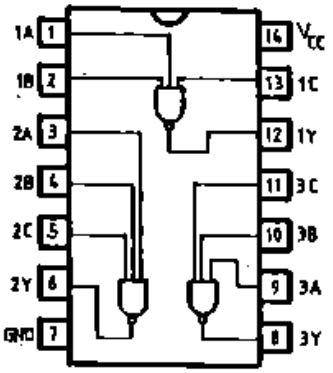


$Y = A.B.C$

PACKAGE TO-116 / TOP VIEW

TRIPLE 3-INPUT NAND GATES WITH OPEN-COLLECTOR OUTPUTS

* 54 LS 12
74 LS 12



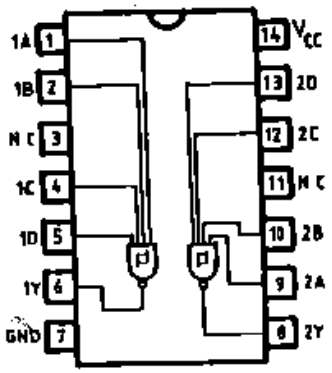
$Y = \overline{A.B.C}$

PACKAGE TO-116 / TOP VIEW

* Preliminary data

DUAL 4-INPUT NAND
SCHMITT TRIGGERS

CDB 413 EM
CDB 413 E

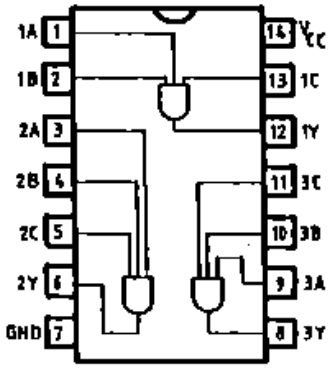


$Y = \overline{A.B.C.D}$

PACKAGE TO-116 / TOP VIEW

TRIPLE 3-INPUT AND GATES
WITH OPEN-COLLECTOR OUTPUTS

*** 54 LS 15**
74 LS 15

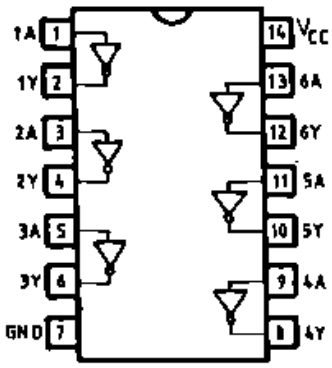


$Y = \overline{A.B.C}$

PACKAGE TO-116 / TOP VIEW

HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS (15 V)

CDB 416 EM
CDB 416 E



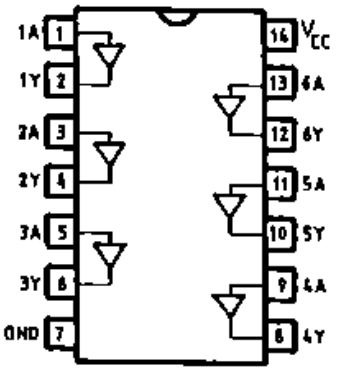
$Y = \overline{A}$

PACKAGE TO-116 / TOP VIEW

* Preliminary data

HEX BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS (15 V)

CDB 417 EM
CDB 417 E



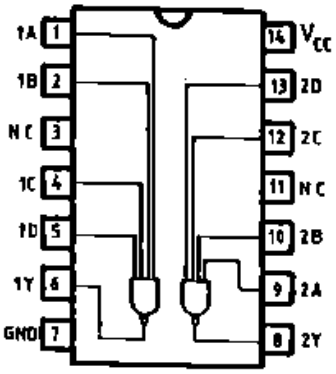
Y = A

PACKAGE TO-116 / TOP VIEW

DUAL 4-INPUT NAND GATES

CDB 420 EM
CDB 420 E

$ 54 LS 20
74 LS 20

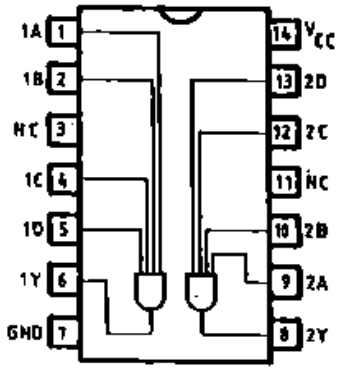


$Y = \overline{A.B.C.D}$

PACKAGE TO-116 / TOP VIEW

DUAL 4-INPUT AND GATES

$ 54 LS 21
74 LS 21



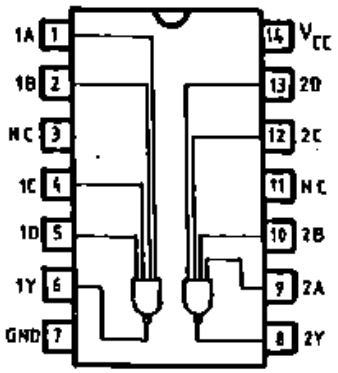
Y = A.B.C.D

PACKAGE TO-116 / TOP VIEW

$ Preliminary data

DUAL 4-INPUT NAND GATES WITH OPEN-COLLECTOR OUTPUTS

* 54 LS 22
74 LS 22

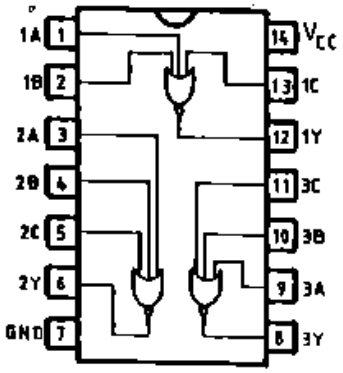


$Y = \overline{A.B.C.D}$

PACKAGE TO-116 / TOP VIEW

TRIPLE 3-INPUT NOR GATES

* 54 LS 27
74 LS 27

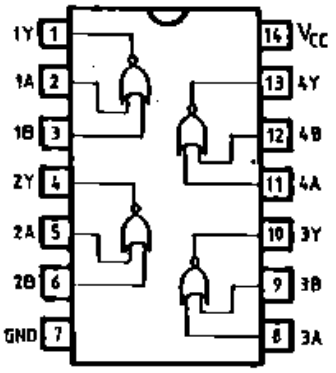


$Y = \overline{A+B+C}$

PACKAGE TO-116 / TOP VIEW

QUADRUPLE 2-INPUT NOR BUFFERS

* 54 LS 28
* 74 LS 28



$Y = \overline{A+B}$

PACKAGE TO-116 / TOP VIEW

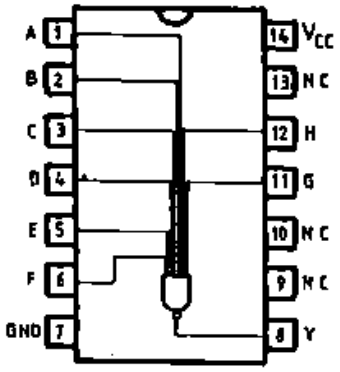
* Preliminary data

8-INPUT NAND GATES

CDB 430 EM
CDB 430 E

CDB 430 HEM
CDB 430 HE

* 54 LS 30
74 LS 30



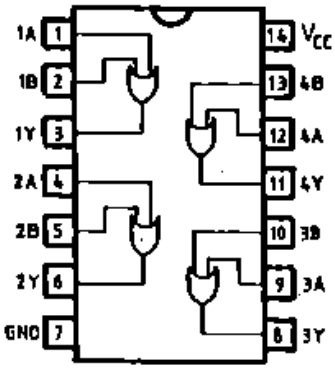
$Y = \overline{A.B.C.D.E.F.G.H}$

PACKAGE TO-116 / TOP VIEW

QUADRUPLE 2-INPUT OR GATES

CDB 432 EM
CDB 432 E

* 54 LS 32
74 LS 32

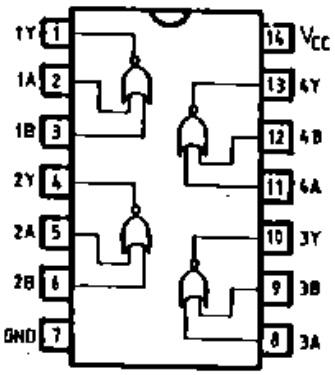


$Y = A+B$

PACKAGE TO-116 / TOP VIEW

QUADRUPLE 2-INPUT NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

* 54 LS 33
* 74 LS 33



$Y = \overline{A+B}$

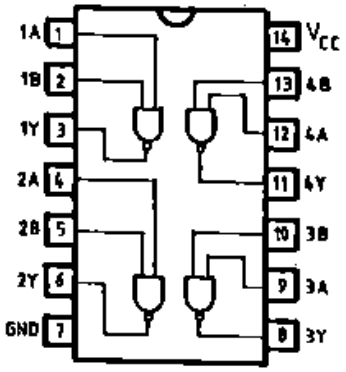
PACKAGE TO-116 / TOP VIEW

* Preliminary data

QUADRUPLE 2-INPUT NAND BUFFERS

CDB 437 EM
CDB 437 E

$ 54 LS 37
$ 74 LS 37



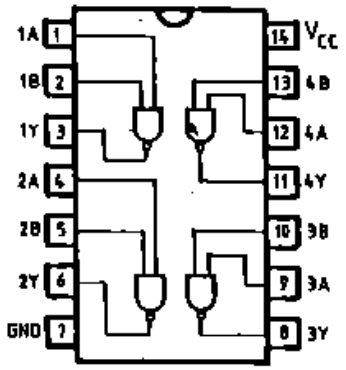
$Y = \overline{A.B}$

PACKAGE TO-116 / TOP VIEW

QUADRUPLE 2-INPUT NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

CDB 438 EM
CDB 438 E

$ 54 LS 38
$ 74 LS 38



$Y = \overline{A.B}$

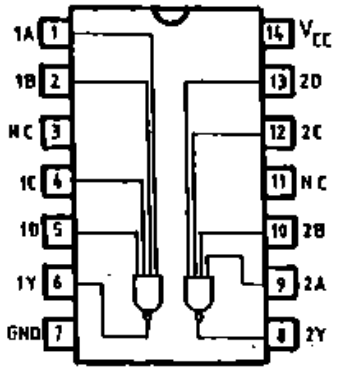
PACKAGE TO-116 / TOP VIEW

DUAL 4-INPUT NAND BUFFERS

CDB 440 EM
CDB 440 E

CDB 440 HEM
CDB 440 HE

$ 54 LS 40
$ 74 LS 40



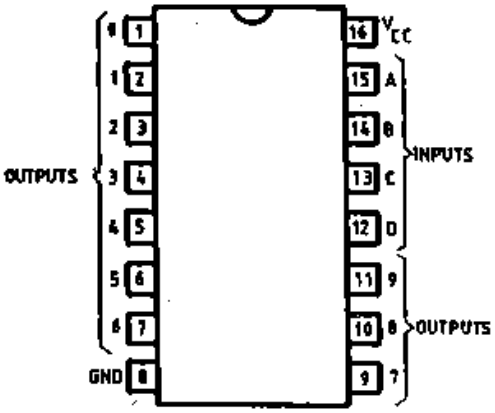
$Y = \overline{A.B.C.D}$

PACKAGE TO-116 / TOP VIEW

$ Preliminary data

4 LINE-TO-10 LINE DECODERS
(BCD-TO-DECIMAL)

CDB 442 EM
CDB 442 E

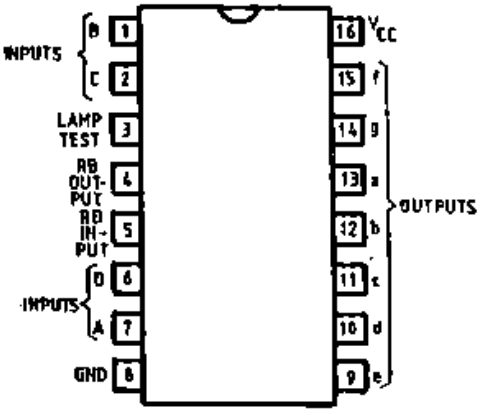


PACKAGE MP-117 / TOP VIEW

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS ACTIVE-LOW, OPEN-COLLECTOR, 30 V OUTPUTS

CDB 446 EM
CDB 446 E

```
        a
       ---
   f / g   / b
       ---
  e /     / c
     ---
       d
```

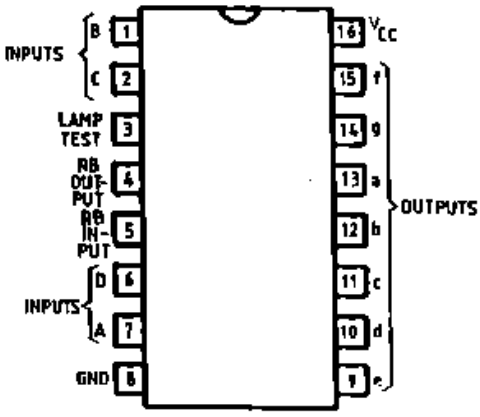


PACKAGE MP-117 / TOP VIEW

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS ACTIVE-LOW, OPEN-COLLECTOR, 15 V OUTPUTS

CDB 447 EM
CDB 447 E

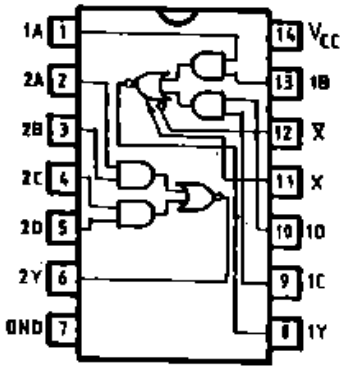
```
        a
       ---
   f / g   / b
       ---
  e /     / c
     ---
       d
```



PACKAGE MP-117 / TOP VIEW

DUAL 2-WIDE 2-INPUT
AND-OR-INVERT GATES
(ONE GATE EXPANDABLE)

CDB 450 EM
CDB 450 E



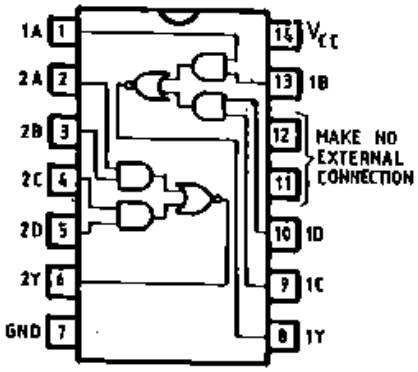
$Y = \overline{A.B+C.D+X}$
X = output of CDB 460 EM/E

PACKAGE TO-116 / TOP VIEW

DUAL 2-WIDE 2-INPUT
AND-OR-INVERT GATES

CDB 451 EM
CDB 451 E

CDB 451 HEM
CDB 451 HE

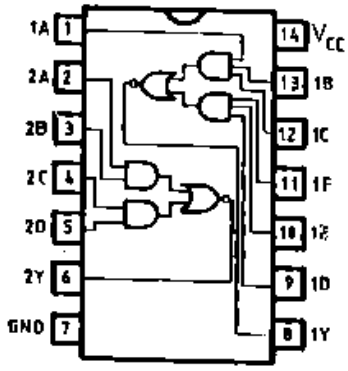


$Y = \overline{A.B+C.D}$

PACKAGE TO-116 / TOP VIEW

2-WIDE 3-INPUT, 2-WIDE 2-INPUT
AND-OR-INVERT GATES

*** 54 LS 51**
74 LS 51



$1Y = \overline{(1A.1B.1C.)+(1D.1E.1F)}$

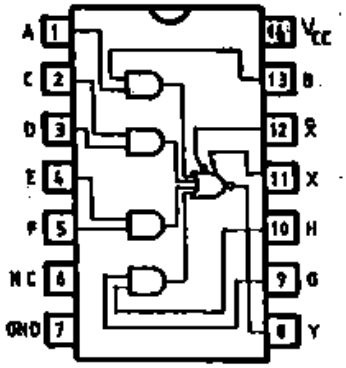
$2Y = \overline{(2A.2B)+(2C.2D)}$

PACKAGE TO-116 / TOP VIEW

* Preliminary data

EXPANDABLE 4-WIDE
AND-OR-INVERT GATES

CDB 453 EM
CDB 453 E

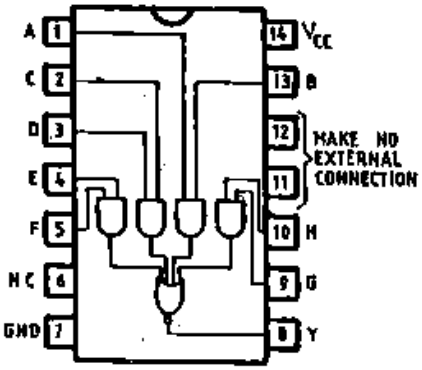


$Y = \overline{A.B+C.D+E.F+G.H+X}$
X = output of CDB 460 EM/E

PACKAGE TO-116 / TOP VIEW

4-WIDE 2-INPUT
AND-OR-INVERT GATES

CDB 454 EM
CDB 454 E

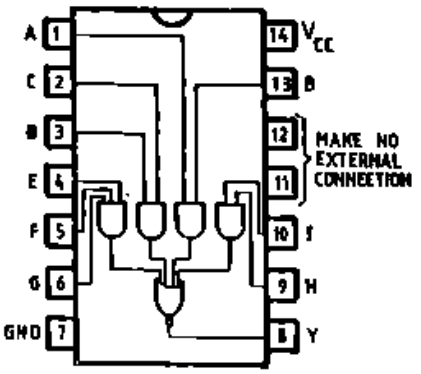


$Y = \overline{A.B+C.D+E.F+G.H}$

PACKAGE TO-116 / TOP VIEW

3-WIDE 2-INPUT + ONE 3-INPUT
AND-OR-INVERT GATES

CDB 454 HEM
CDB 454 HE

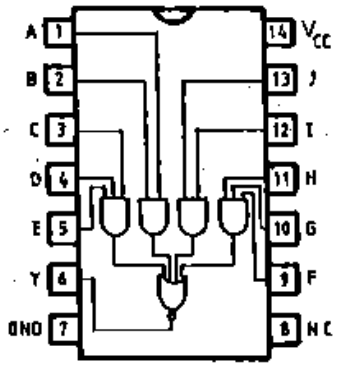


$Y = \overline{A.B+C.D+E.F.G.+H.I}$

PACKAGE TO-116 / TOP VIEW

2-WIDE 2-INPUT, 2-WIDE 3-INPUT AND-OR-INVERT GATES

* 54 LS 54
74 LS 54

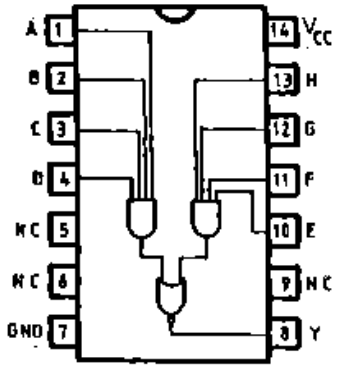


$Y = \overline{A.B+C.D.E+F.G.H+I.J}$

PACKAGE TO-116 / TOP VIEW

2-WIDE 4-INPUT AND-OR-INVERT GATES

* 54 LS 55
74 LS 55

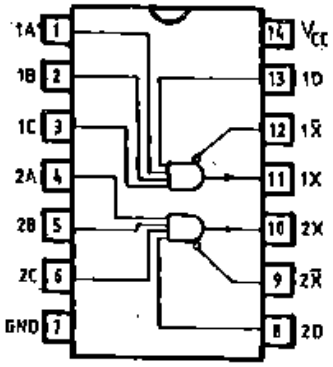


$Y = \overline{A.B.C.D+E.F.G.H}$

PACKAGE TO-116 / TOP VIEW

DUAL 4-INPUT EXPANDERS

CDB 460 EM
CDB 460 E



X = A.B.C.D when connected to X and $\overline{X}$ inputs of CDB 450 or CDB 453 (EM/E)

PACKAGE TO-116 / TOP VIEW

* Preliminary data

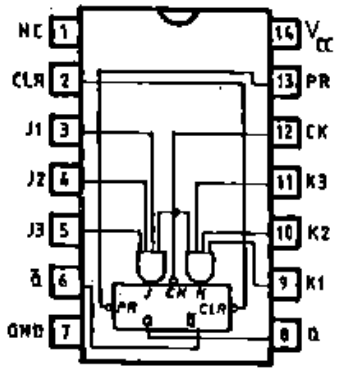
AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

CDB 472 EM
CDB 472 E

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	1	1
1	1	⎍	0	0	Q0	$\bar{Q}$0
1	1	⎍	1	0	1	0
1	1	⎍	0	1	0	1
1	1	⎍	1	1	TOGGLE	

J = J1.J2.J3; K = K1.K2.K3



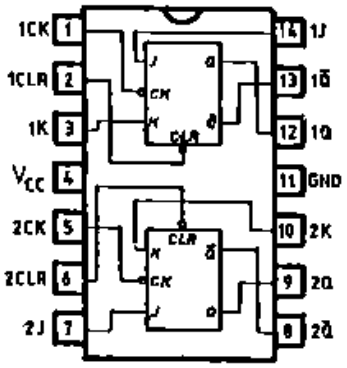
PACKAGE TO-116 / TOP VIEW

DUAL J-K FLIP-FLOPS WITH CLEAR

CDB 473 EM
CDB 473 E

FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
0	X	X	X	1	0
1	⎍	0	0	Q0	$\bar{Q}$0
1	⎍	1	0	1	0
1	⎍	0	1	0	1
1	⎍	1	1	TOGGLE	



PACKAGE TO-116 / TOP VIEW

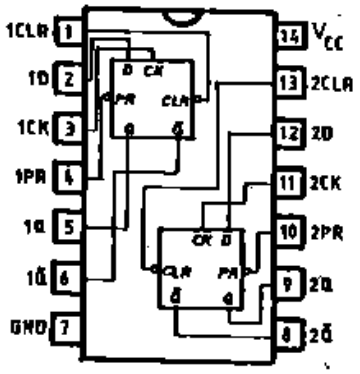
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

CDB 474 EM
CDB 474 E

$ 54 LS 74
$ 74 LS 74

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1	1
1	1	↑	1	1	0
1	1	↑	0	0	1
1	1	0	X	Q0	$\bar{Q}$0



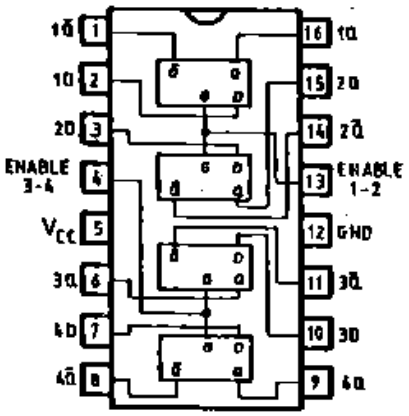
PACKAGE TO-116 / TOP VIEW

4-BIT BISTABLE LATCHES

CDB 475 EM
CDB 475 E

FUNCTION TABLE
(EACH LATCH)

INPUTS		OUTPUTS	
D	G	Q	$\bar{Q}$
0	1	0	1
1	1	1	0
X	0	Q0	$\bar{Q}$0



PACKAGE MP-117 / TOP VIEW

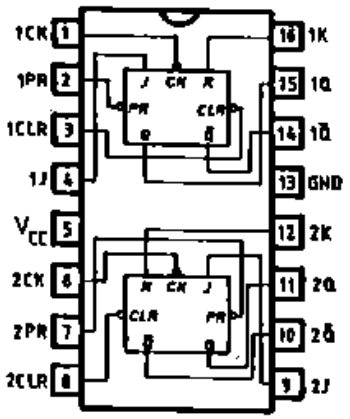
$ Preliminary data

DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

CDB 476 EM
CDB 476 E

FUNCTION TABLE

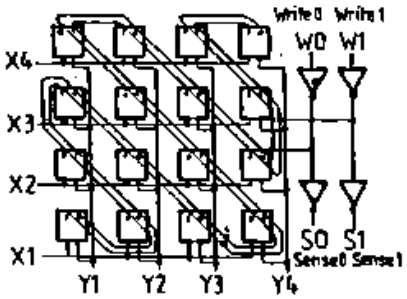
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	1	1
1	1	⎍	0	0	Q0	$\bar{Q}$0
1	1	⎍	1	0	1	0
1	1	⎍	0	1	0	1
1	1	⎍	1	1	TOGGLE	

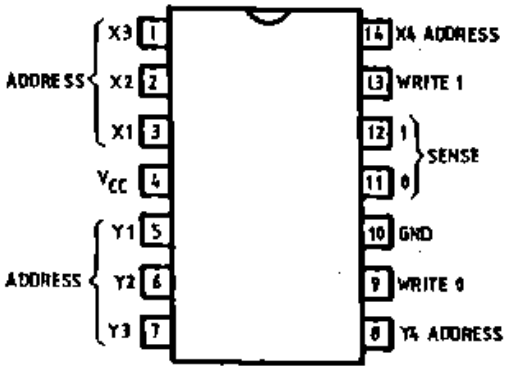


PACKAGE MP-117 / TOP VIEW

16-BIT RANDOM-ACCESS MEMORIES

CDB 481 EM
CDB 481 E

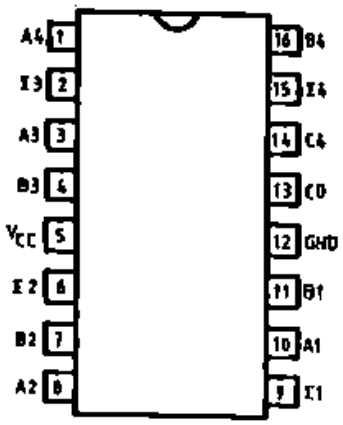




PACKAGE TO-116 / TOP VIEW

4-BIT BINARY FULL ADDERS WITH FAST CARRY

CDB 483 EM
CDB 483 E



PACKAGE MP-117 / TOP VIEW

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

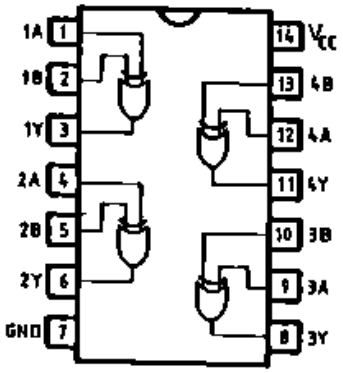
CDB 486 EM
CDB 486 E

*** 54 LS 86**
*** 74 LS 86**

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

$Y = A \oplus B = \overline{A.B}+\overline{A.B}$

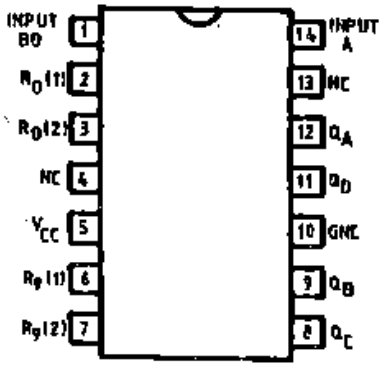


PACKAGE TO-116 / TOP VIEW

* Preliminary data

DECADE COUNTERS
(DIVIDE-BY-TWO AND
DIVIDE-BY-FIVE)

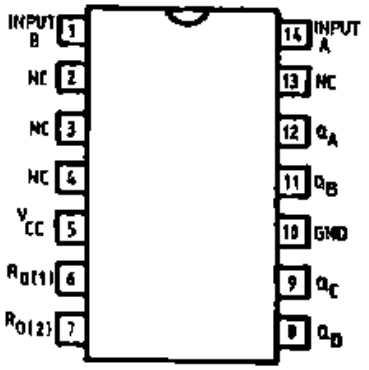
CDB 490 EM
CDB 490 E



PACKAGE TO-116 / TOP VIEW

DIVIDE-BY-TWELVE COUNTERS
(DIVIDE-BY-TWO AND
DIVIDE-BY-SIX)

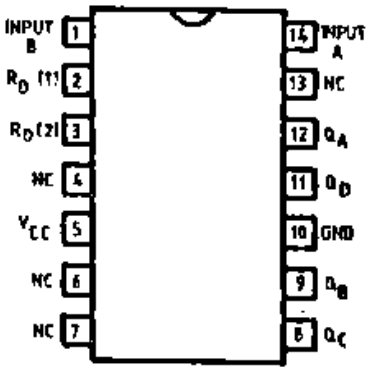
CDB 492 EM
CDB 492 E



PACKAGE TO-116 / TOP VIEW

4-BIT BINARY COUNTERS
(DIVIDE-BY-TWO AND
DIVIDE-BY-EIGHT)

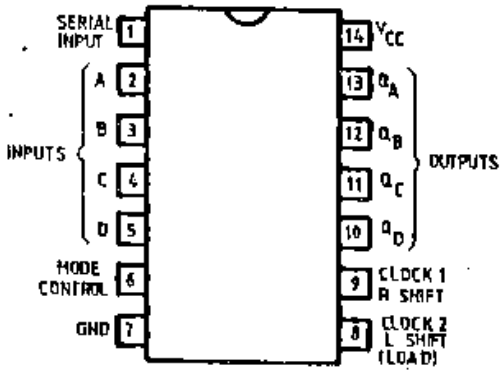
CDB 493 EM
CDB 493 E



PACKAGE TO-116 / TOP VIEW

4-BIT SHIFT REGISTERS
(PARALLEL IN/PARALLEL OUT, SHIFT RIGHT, SHIFT LEFT, SERIAL INPUT

CDB 495 EM
CDB 495 E



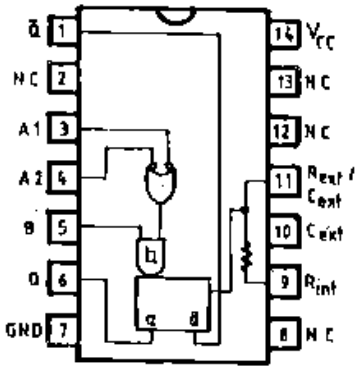
PACKAGE TO-116 / TOP VIEW

MONOSTABLE MULTIVIBRATORS

CDB 4121 EM
CDB 4121 E

FUNCTION TABLE

INPUTS			OUTPUTS	
A1	A2	B	Q	$\bar{Q}$
0	X	1	0	1
X	0	1	0	1
X	X	0	0	1
1	1	X	0	1
1	↑	1	⎍	⎎
↑	1	1	⎍	⎎
↑	↑	1	⎍	⎎
0	X	↑	⎍	⎎
X	0	↑	⎍	⎎



PACKAGE TO-116 / TOP VIEW

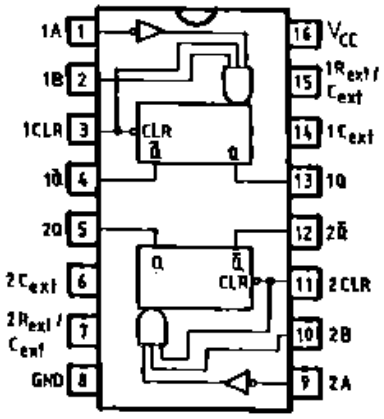
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

CDB 4123 EM
CDB 4123 E

*** 54 LS 123**
*** 74 LS 123**

FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
0	X	X	0	1
X	1	X	0	1
X	X	0	0	1
1	0	↑	⎍	⊔
1	↓	1	⎍	⊔
↑	0	1	⎍	⊔



PACKAGE MP-117 / TOP VIEW

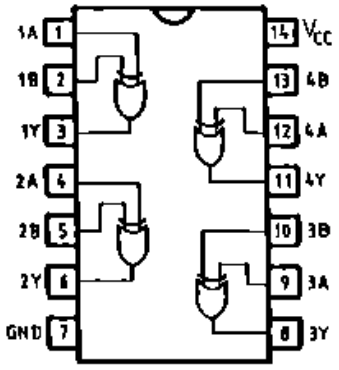
QUAD 2-INPUT EXCLUSIVE-OR GATES WITH-OPEN COLLECTOR OUTPUTS

*** 54 LS 136**
*** 74 LS 136**

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

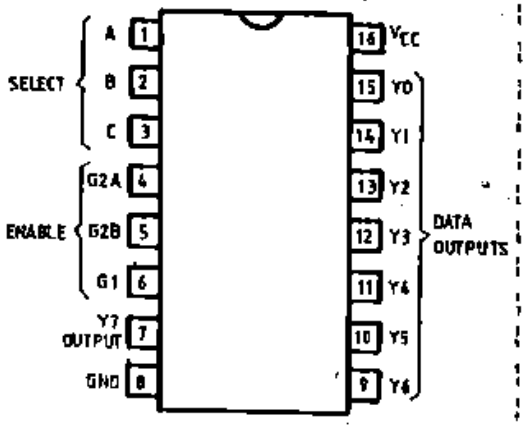
$Y = A \oplus B = A.\bar{B}+\bar{A}.B$



PACKAGE TO-116 / TOP VIEW

3-TO-8 LINE DECODERS/MULTIPLEXERS

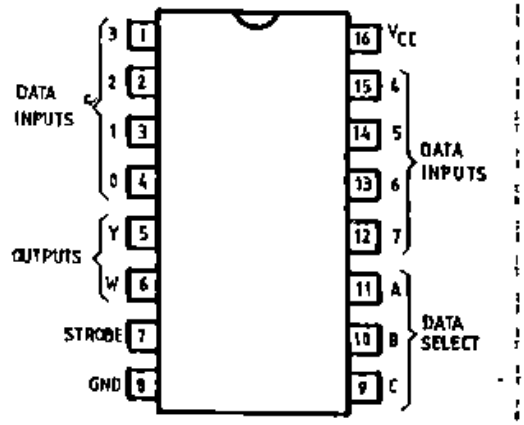
$ 54 LS 138
$ 74 LS 138



PACKAGE MP-117 / TOP VIEW

1-OF-8 DATA SELECTORS/MULTIPLEXERS

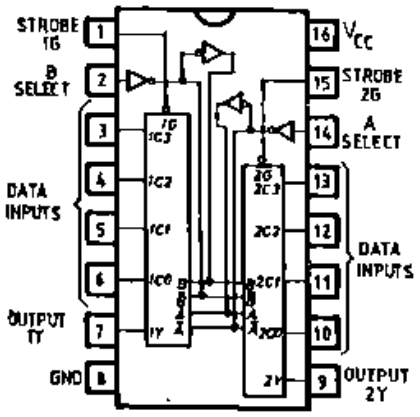
CDB 4151 EM
CDB 4151 E



PACKAGE MP-117 / TOP VIEW

DUAL 4 LINE-TO-1 LINE DATA SELECTORS/MULTIPLEXERS

CDB 4153 EM
CDB 4153 E



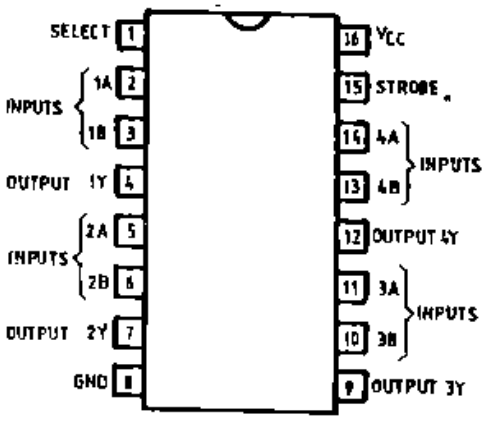
PACKAGE MP-117 / TOP VIEW

$ Preliminary data

QUAD 2-TO-1 LINE
DATA SELECTORS/MULTIPLEXERS
(NONINVERTED DATA OUTPUTS)

CDB 4157 EM
CDB 4157 E

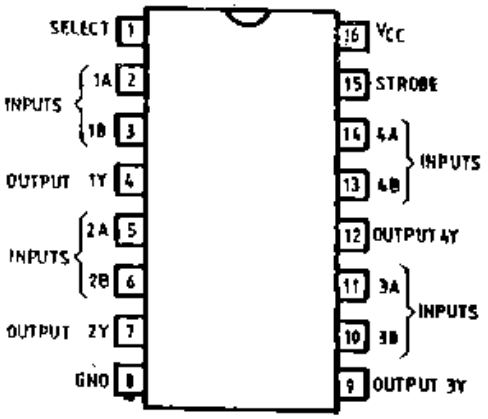
* 54 LS 157
* 74 LS 157



PACKAGE MP-117 / TOP VIEW

QUAD 2-TO-1 LINE
DATA SELECTORS/MULTIPLEXERS
(INVERTED DATA OUTPUTS)

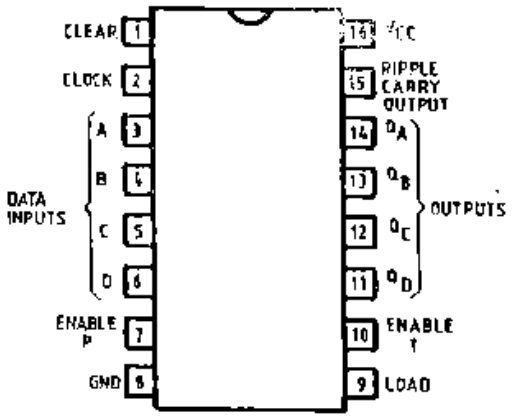
* 54 LS 158
* 74 LS 158



PACKAGE MP-117 / TOP VIEW

SYNCHRONOUS 4-BIT COUNTERS
(DECADE, DIRECT CLEAR)

* 54 LS 160
* 74 LS 160

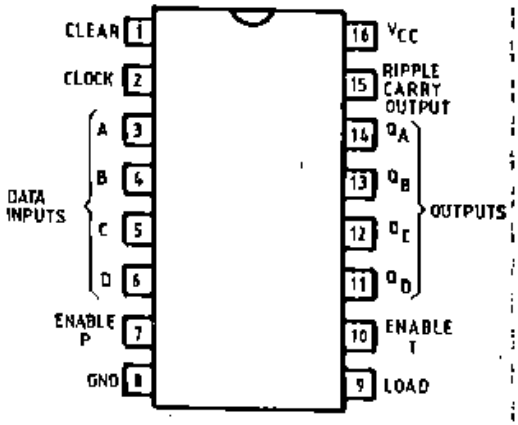


PACKAGE MP-117 / TOP VIEW

* Preliminary data

SYNCHRONOUS 4-BIT COUNTERS
(BINARY, DIRECT CLEAR)

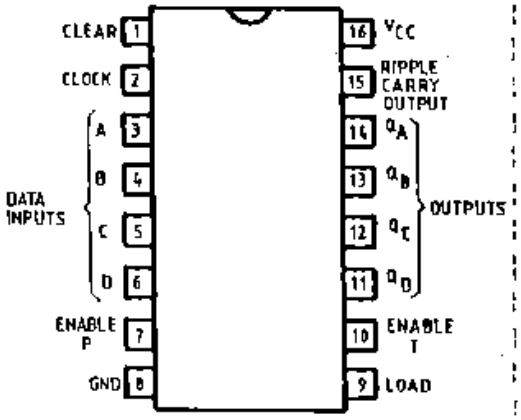
* 54 LS 161
* 74 LS 161



PACKAGE MP-117 / TOP VIEW

SYNCHRONOUS 4-BIT COUNTERS
(DECADE, SYNCHRONOUS CLEAR)

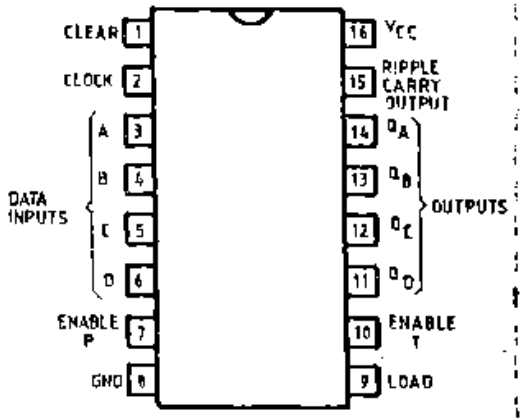
* 54 LS 162
* 74 LS 162



PACKAGE MP-117 / TOP VIEW

SYNCHRONOUS 4-BIT COUNTERS
(BINARY, SYNCHRONOUS CLEAR)

* 54 LS 163
* 74 LS 163

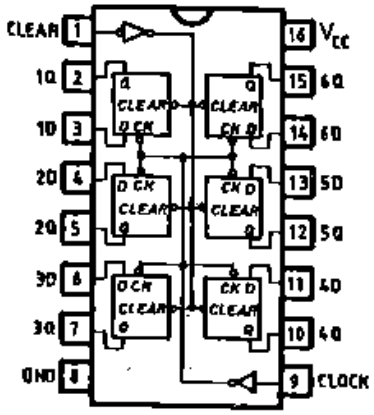


PACKAGE MP-117 / TOP VIEW

* Preliminary data

HEX D-TYPE FLIP-FLOPS
(SINGLE RAIL OUTPUTS
COMMON DIRECT CLEAR)

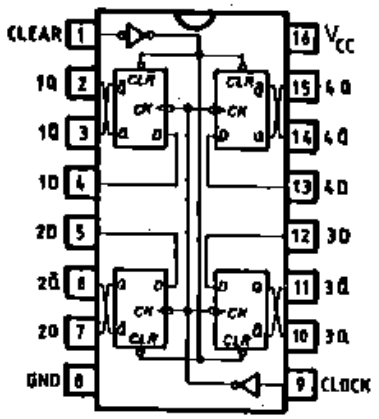
$ 54 LS 174
$ 74 LS 174



PACKAGE MP-117 / TOP VIEW

QUAD D-TYPE FLIP-FLOPS
(COMPLEMENTARY OUTPUTS
COMMON DIRECT CLEAR)

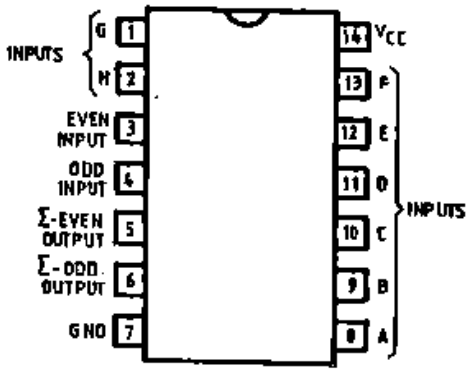
$ 54 LS 175
$ 74 LS 175



PACKAGE MP-117 / TOP VIEW

8-BIT ODD/EVEN PARITY
GENERATORS/CHECKERS

CDB 4180 EM
CDB 4180 E

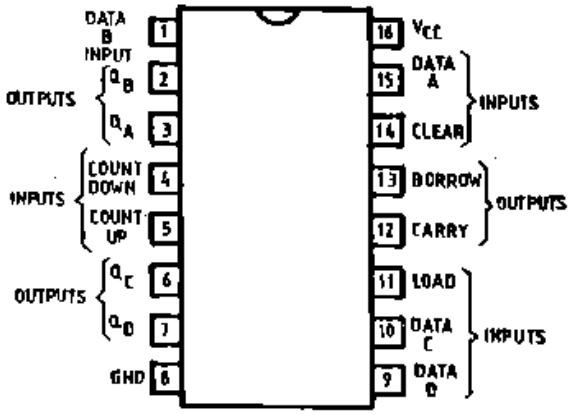


PACKAGE TO-116 / TOP VIEW

$ Preliminary data

SYNCHRONOUS UP/DOWN
DUAL CLOCK COUNTERS
(BCD WITH CLEAR)

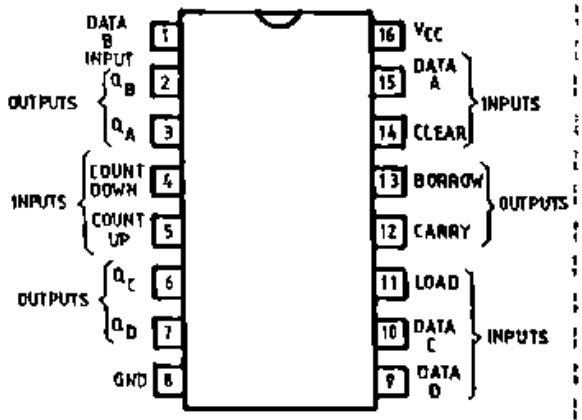
CDB 4192 EM
CDB 4192 E



PACKAGE MP-117 / TOP VIEW

SYNCHRONOUS UP/DOWN
DUAL CLOCK COUNTERS
(BINARY WITH CLEAR)

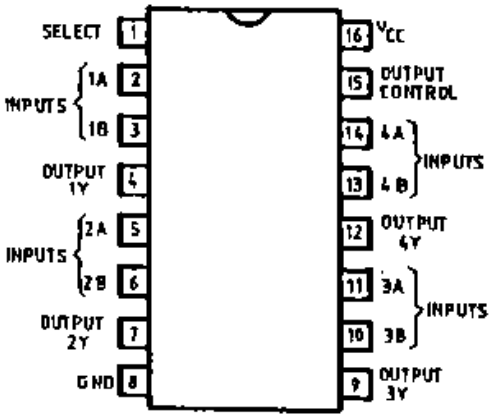
CDB 4193 EM
CDB 4193 E



PACKAGE MP-117 / TOP VIEW

QUAD DATA SELECTORS/MULTIPLEXERS
(NONINVERTED 3-STATE OUTPUTS)

*** 54 LS 257**
*** 74 LS 257**

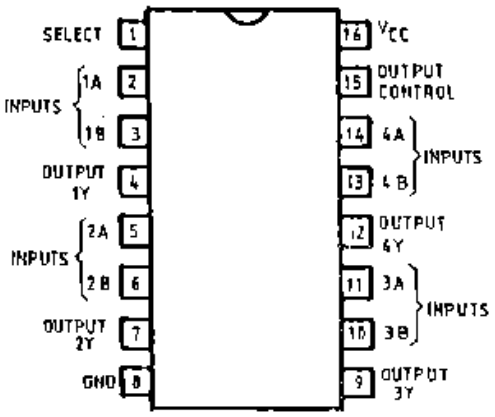


PACKAGE MP-117 / TOP VIEW

* Preliminary data

QUAD DATA SELECTORS/MULTIPLEXERS
(INVERTED 3-STATE OUTPUTS)

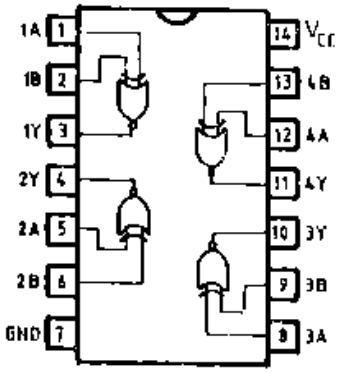
* 54 LS 258
* 74 LS 258



PACKAGE MP-117 / TOP VIEW

QUAD 2-INPUT EXCLUSIVE-NOR GATES
WITH OPEN-COLLECTOR OUTPUTS

* 54 LS 266
* 74 LS 266

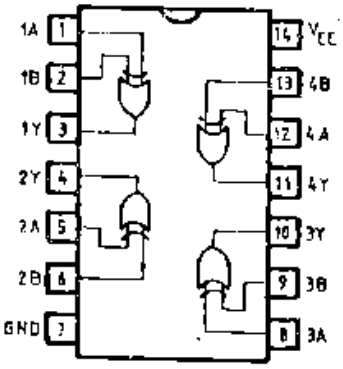


$Y = \overline{A \oplus B} = \overline{A.B+A.B}$

PACKAGE TO-116 / TOP VIEW

QUAD 2-INPUT EXCLUSIVE-OR GATES

* 54 LS 386
* 74 LS 386



$Y = A \oplus B = A.\overline{B}+\overline{A}B$

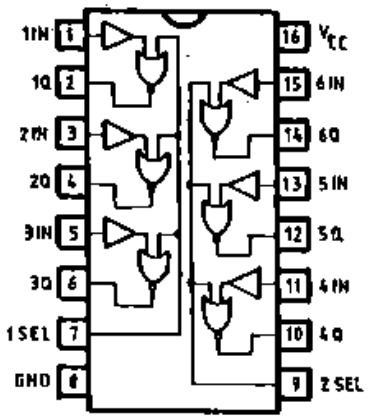
PACKAGE TO-116 / TOP VIEW

* Preliminary data

HEX UNIFIED BUS RECEIVERS

*** CDB 837 EM**
CDB 837 E
CDB 837 EA

TYPE	/	tPLHmax
CDB 837 EM		30 ns
CDB 837 E		30 ns
CDB 837 EA		50 ns

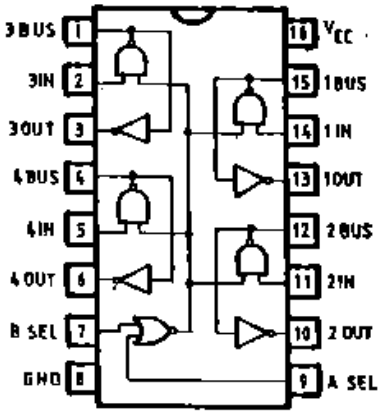


PACKAGE MP-117 / TOP VIEW

QUAD UNIFIED BUS TRANSCEIVERS

*** CDB 838 EM**
CDB 838 E
CDB 838 EA

TYPE	/	tPLHmax
CDB 838 EM		30 ns
CDB 838 E		30 ns
CDB 838 EA		40 ns

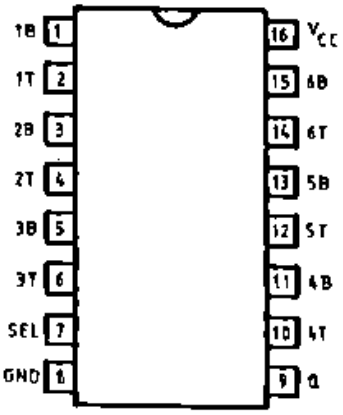


PACKAGE MP-117 / TOP VIEW

6-BIT COMPARATORS

CDB 8136 E
CDB 8136 C

TYPE	/	tPLHmax
CDB 8136 E		45 ns
CDB 8136 C		60 ns



PACKAGE MP-117 / TOP VIEW

* Preliminary data